

(PRIOR ART)

FIG. 34

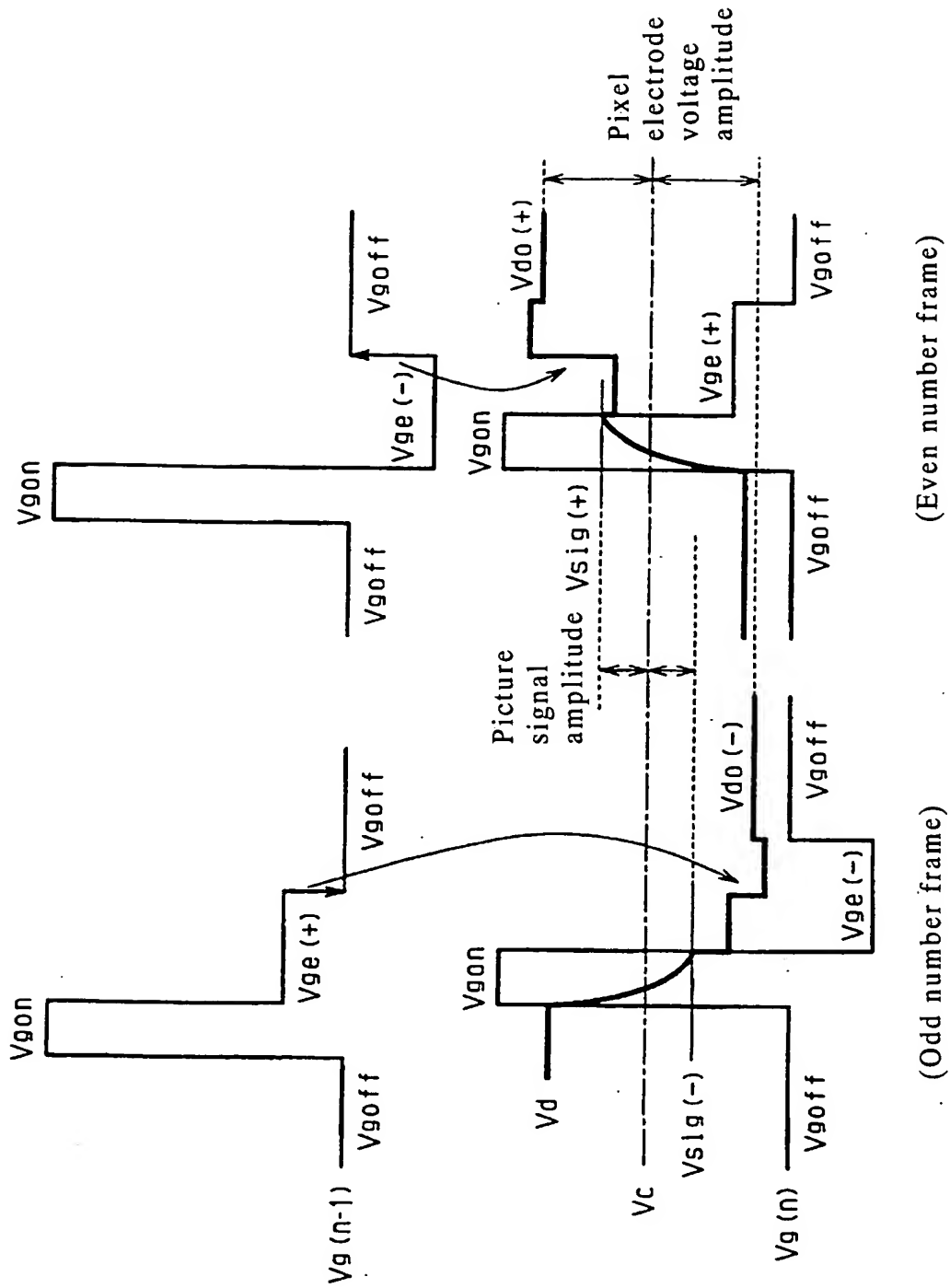


FIG. 35 (PRIOR ART)

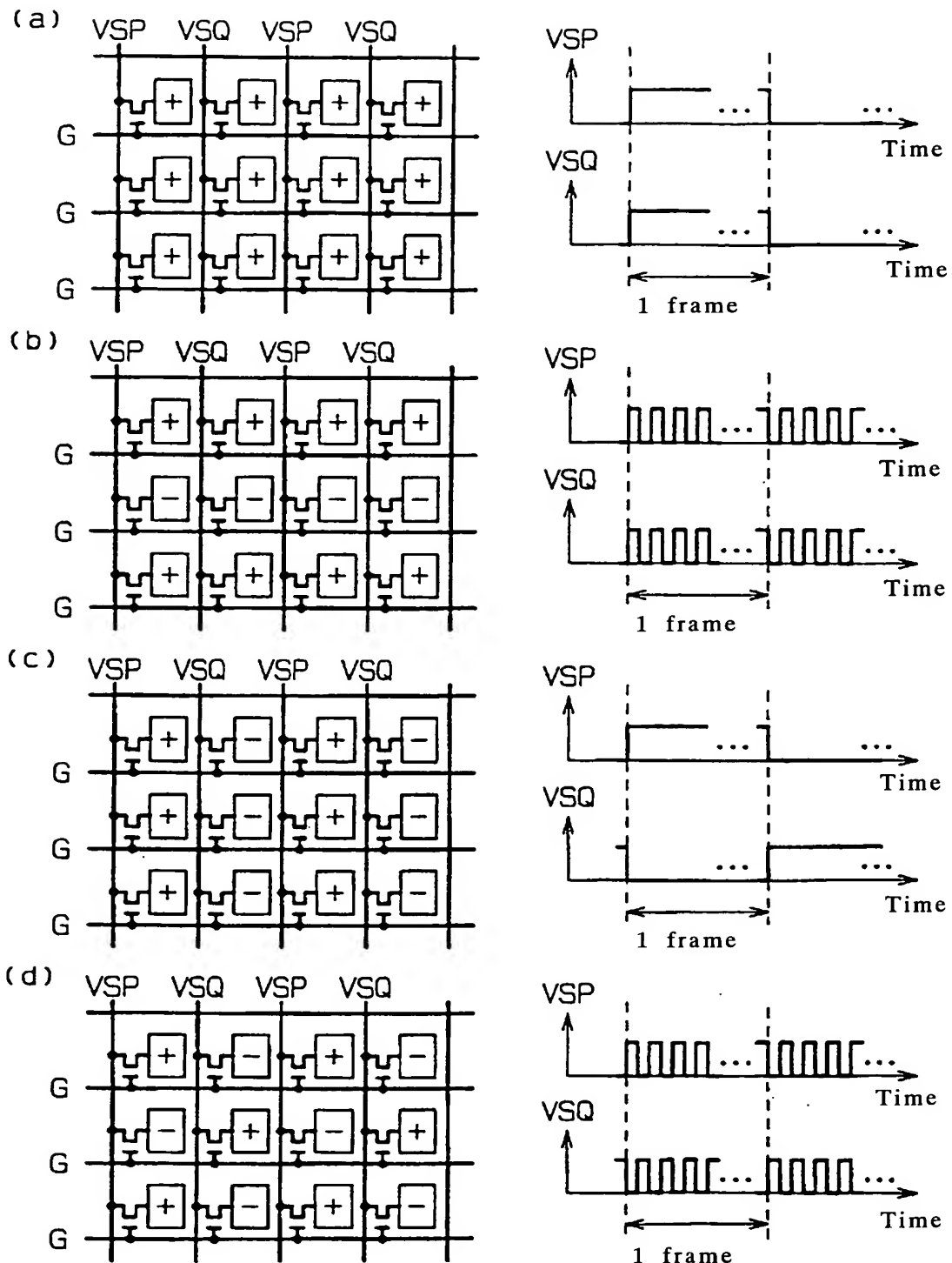
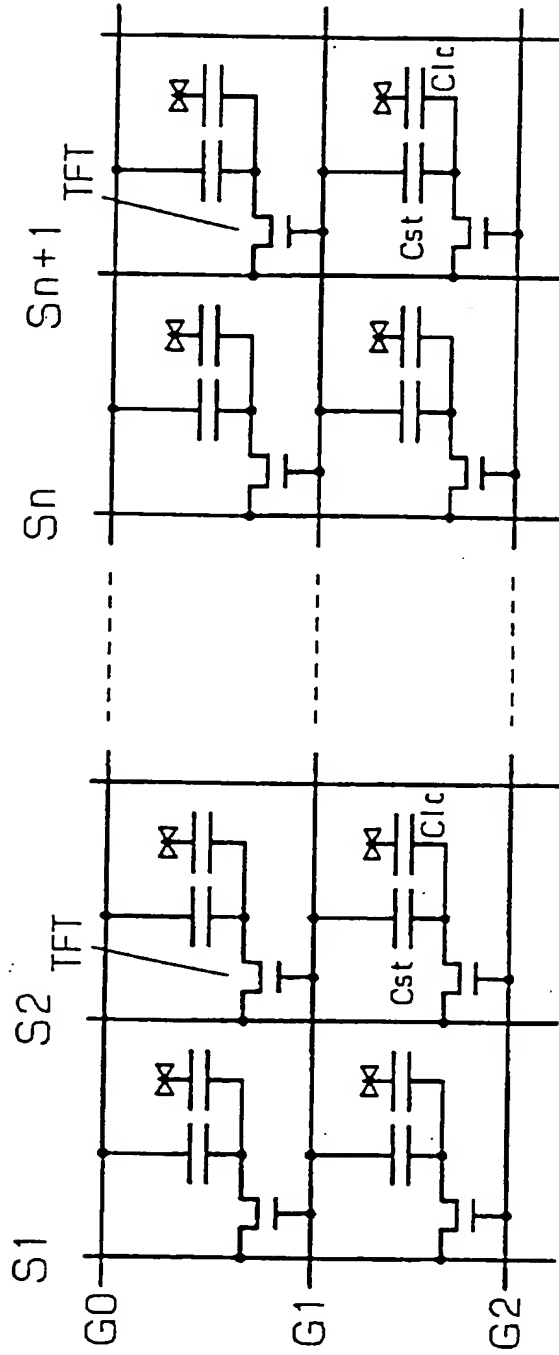


FIG. 36 (PRIOR ART)



(PRIOR ART)

FIG. 37

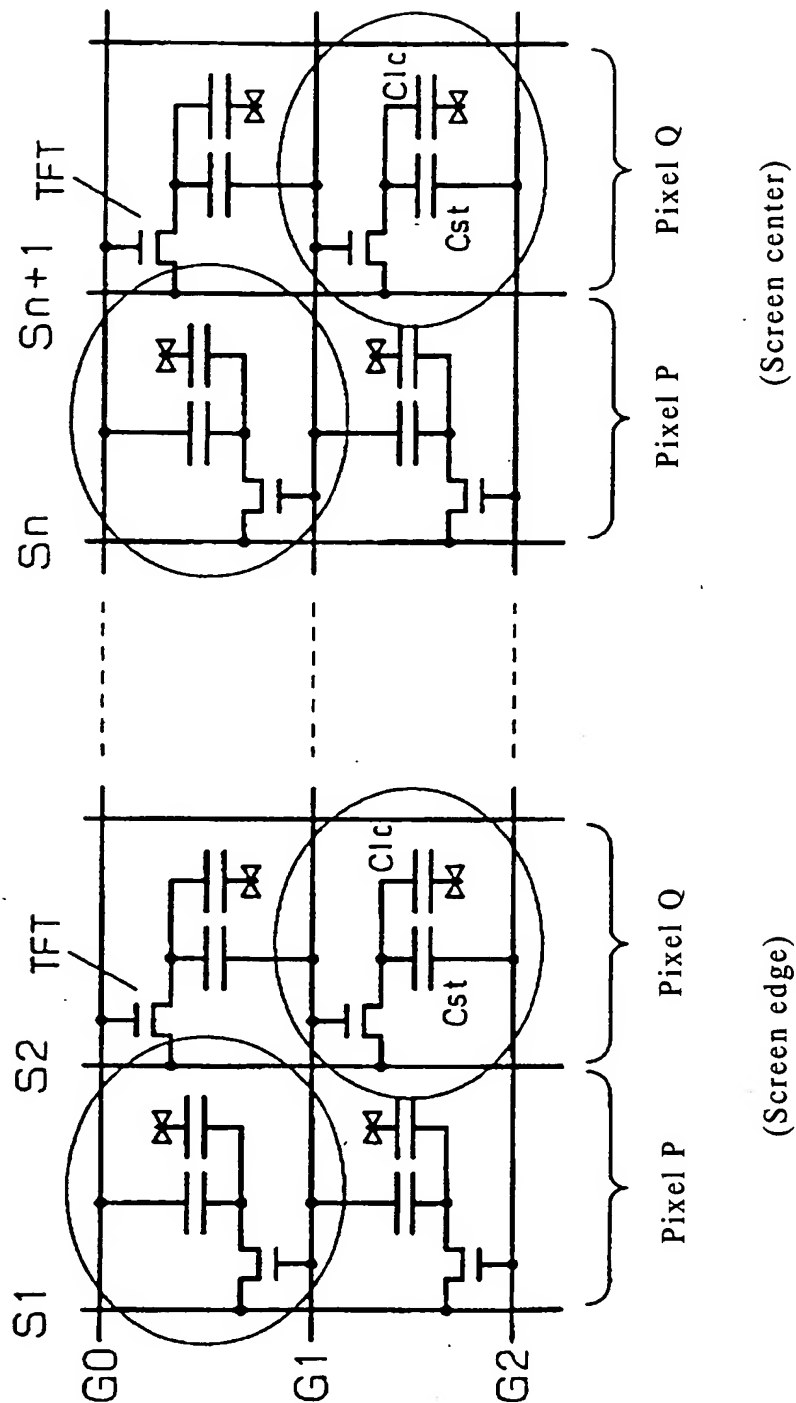


FIG. 38 (PRIOR ART)

FIG. 39

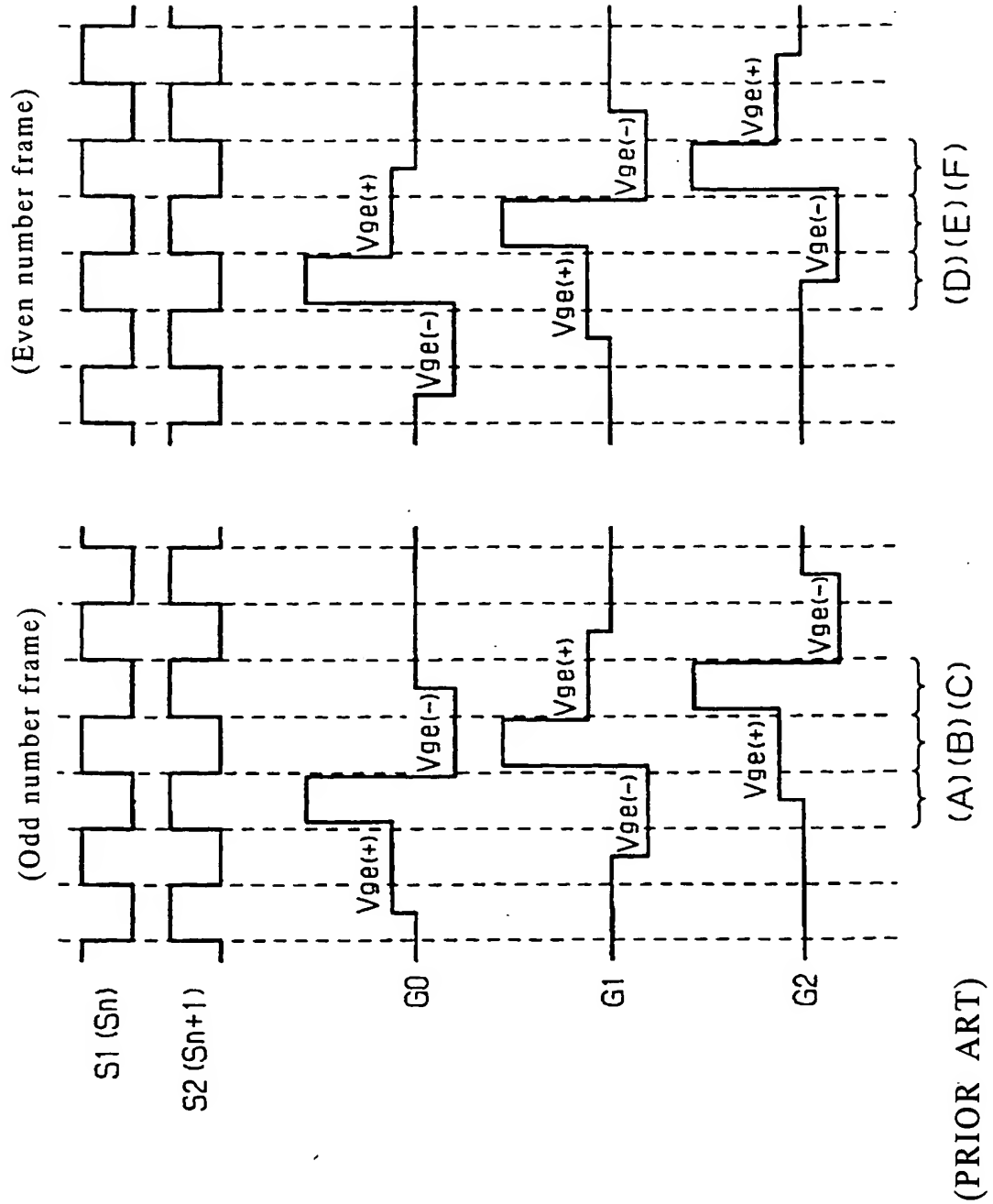


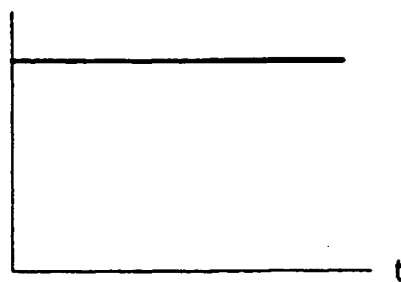
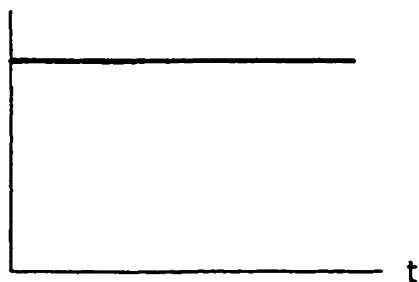
FIG. 39

(Power feeding edge)

(Terminal edge)

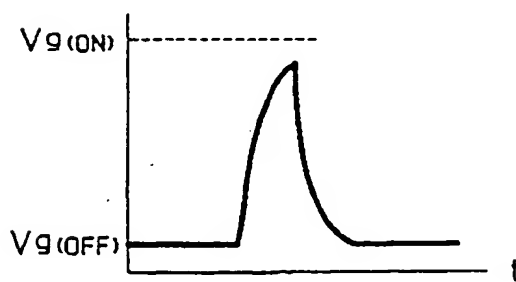
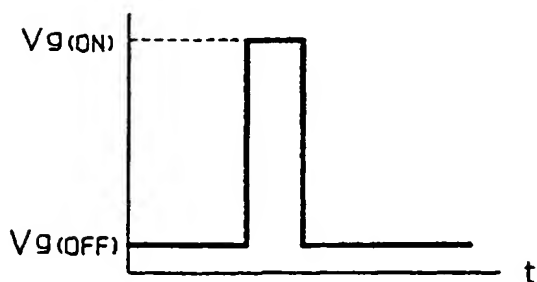
Source voltage

Source voltage



Gate voltage

Gate voltage



Pixel voltage

Pixel voltage

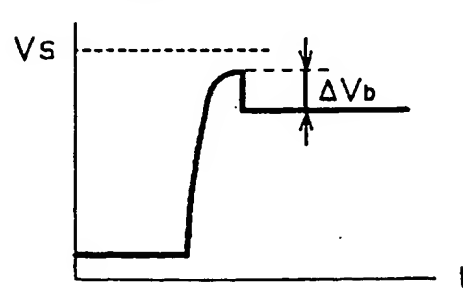
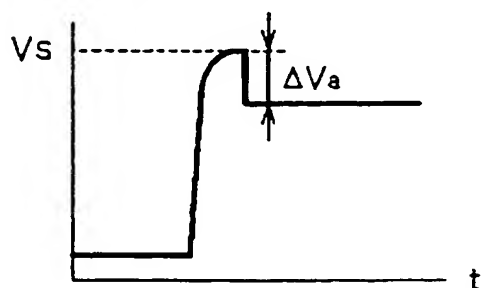


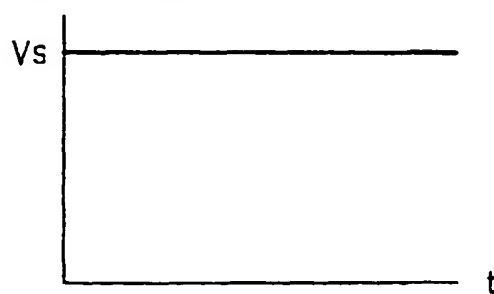
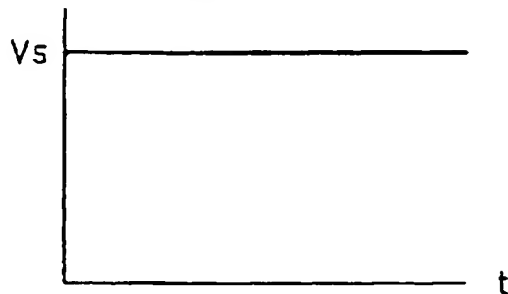
FIG. 40 (PRIOR ART)

(Power feeding edge)

(Terminal edge)

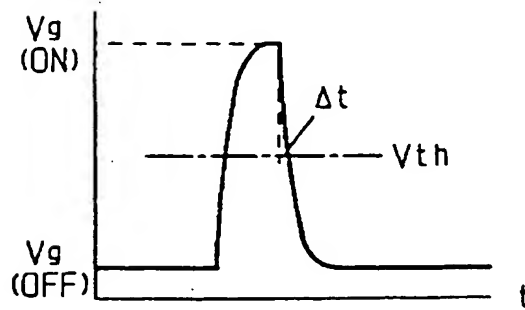
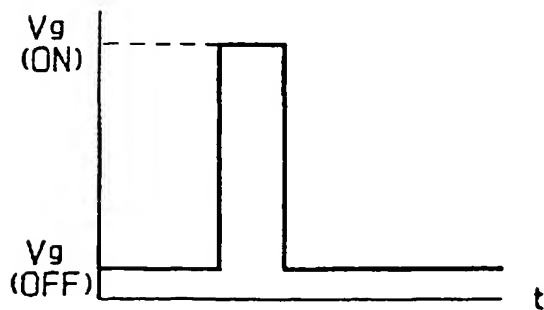
Source voltage

Source voltage



Gate voltage

Gate voltage



Pixel voltage

Pixel voltage

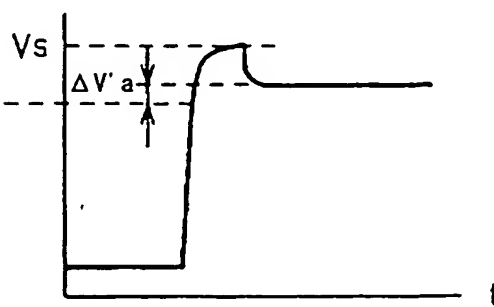
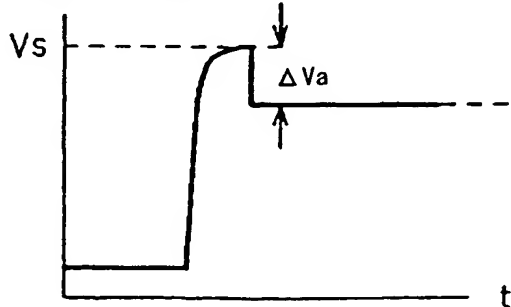


FIG. 41 (PRIOR ART)



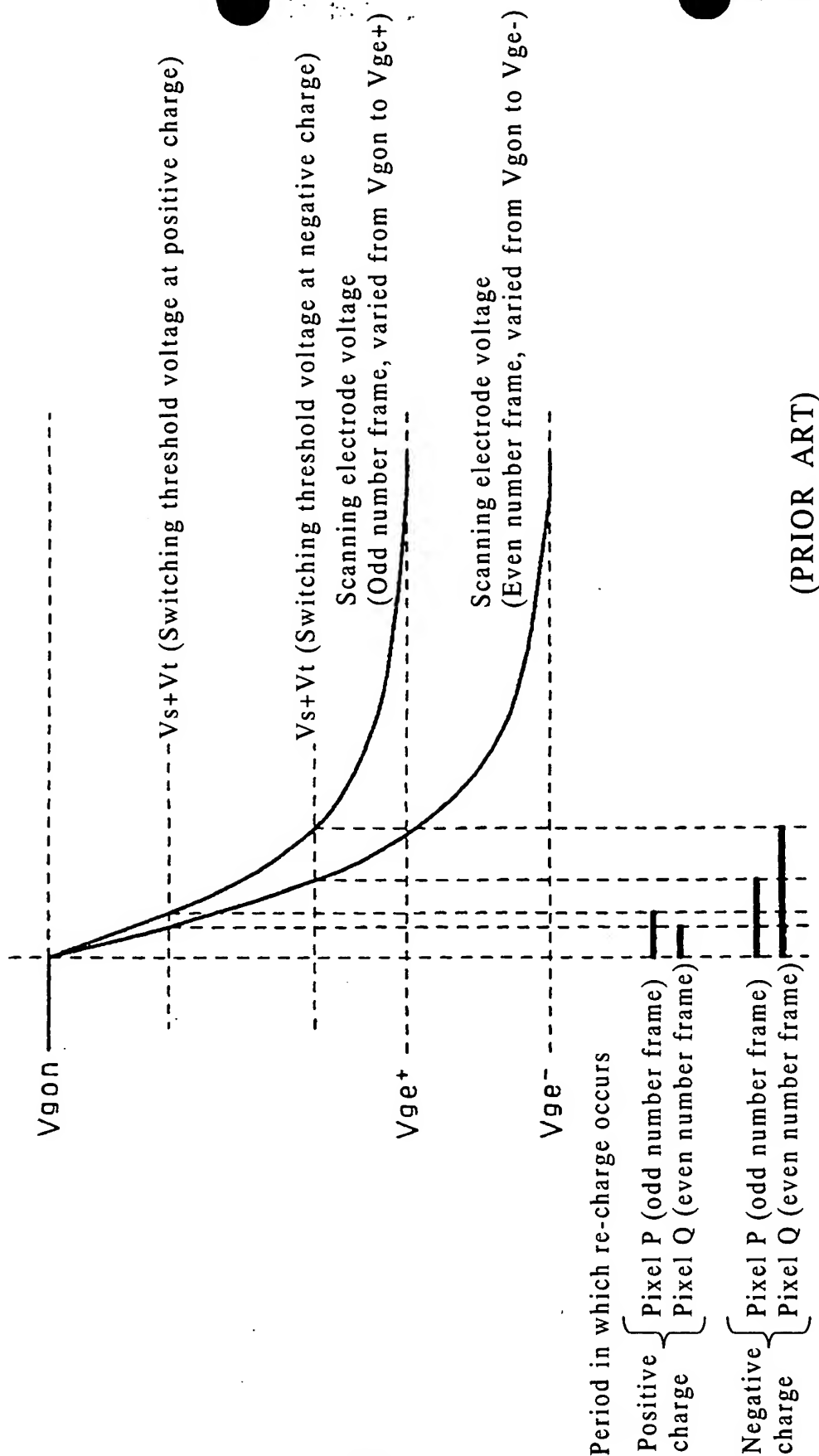


FIG. 42

(Terminal edge)

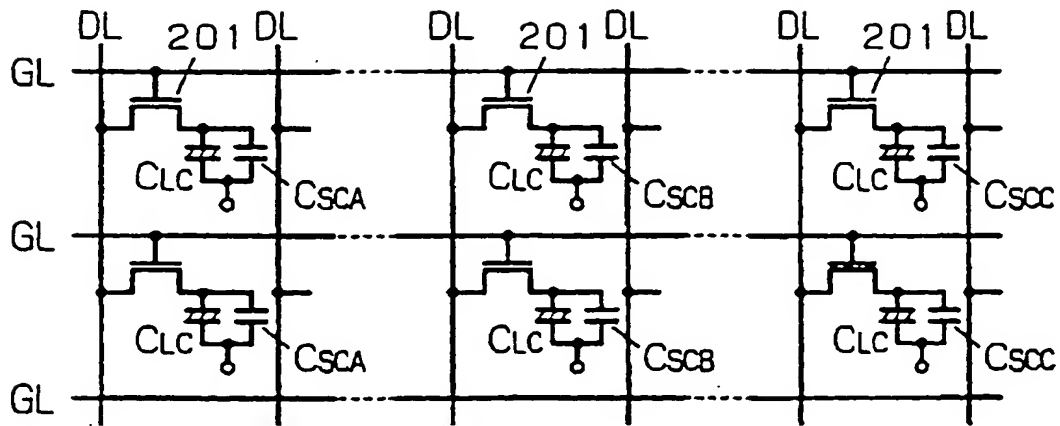
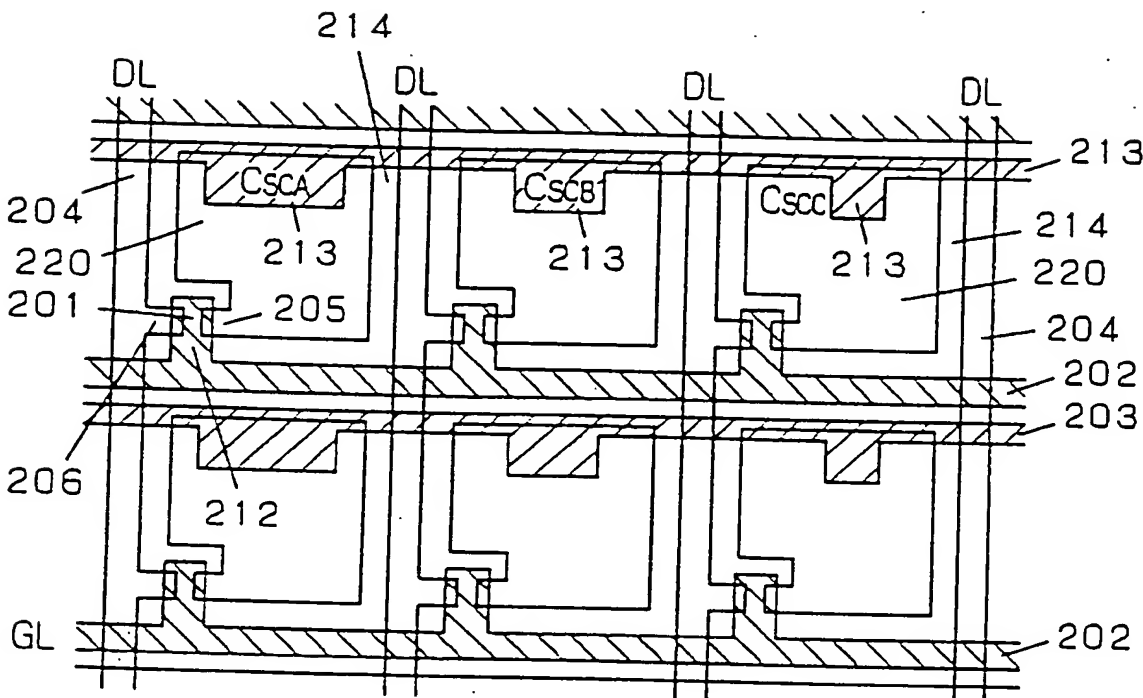


FIG. 43 (PRIOR ART)



(PRIOR ART)

FIG. 44